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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/816,480	03/26/2001	Kazuyoshi Kohno	205127US2	6414

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EXAMINER	
CHANG, SUNRAY	
ART UNIT	**PAPER NUMBER**
2121	5

DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/816,480	Applicant(s) KOHNO ET AL.	
	Examiner Sunray Chang	Art Unit 2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 16 are presented for examination.

Claims 1 – 16 are rejected.

Priority

2. Should applicant desire to obtain the benefit of foreign priority under 35 U.S.C. 119(a)-(d) prior to declaration of an interference, a translation of the foreign application should be submitted under 37 CFR 1.55 in reply to this action.

3. Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. **Claims 1 – 16 are rejected** under 35 U.S.C. 103(a) as being unpatentable over Warren G. Stapleton (U.S. Patent No. 5,870,585, and referred to as Stapleton hereinafter), and in view of Graham R. Hellestrand et al. (U.S. Patent No. 6,230,114, and referred to as Hellestrand hereinafter).

5. **Regarding independent claim 1**:

- **Generating verification programs** by a computer based on a pipeline specification of a **microprocessor as a target in design described in a description language readable and analyzable by a computer**;

  Stapleton teaches a "106 CONVERT TO VERILOG MODEL" block [**generating verification programs**] based on "102 C++ MODEL" [**microprocessor as a target in design described in a description language readable and analyzable by a computer**]; (Fig. 1)

- **Executing a simulation** of a **RTL description** of the **microprocessor** based on the **generated verification program** and the **RTL description**;

Stapleton teaches a "107 SIMULATE" **[Executing a simulation]** of the "102 C++ MODEL" **[RTL description of the microprocessor]** based on the "106 CONVERT TO VERILOG MODEL" **[generated verification program]** and the "102 C++ MODEL" **[RTL description]**. (Fig. 1)

Further, Stapleton teaches a register transfer level (RTL) model **[RTL description]** is created using an object-oriented programming language **[C++]**. (Line 1 – 2, Abstract)

- **Generating a pipeline simulator by the computer** based on the **specification**.

Stapleton teaches a "103 COMPILE" block **[Generating a simulator by the computer]** based on "102 C++ MODEL" **[specification]**; (Fig. 1)

- **Executing a pipeline simulation** based on the **verification programs** and the **generated simulator**.

Stapleton teaches a "104 SIMULATE" block **[executing a simulation]** based on "103 COMPILE" **[verification programs]** and "102 C++ MODEL" **[specification]**; (Fig. 1)

- **Comparing a result of the pipeline simulation of the RTL description** and **a result of the simulation**, and **verifying pipeline operation of the microprocessor based on a comparison result**.

Stapleton teaches a "105 VERIFY" [**Comparing**] "104 ↔ 105" [**a result of the simulation of the RTL description**] and "107 ↔ 105" [**a result of the simulation**] and "105 VERIFY" [**verifying**] "104 and 107" [**operation of the microprocessor**] based on a "105 VERIFY" [**comparison result**]. (Fig. 1)

Stapleton does not teach **pipeline specification** and **pipeline simulator**.

Hellestrand teaches pipeline characteristics (17, Fig. 1) [**pipeline specification**] and pipeline simulator (611, Fig. 6) [**pipeline simulator**]

It would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Stapleton to include "pipeline specification and pipeline simulator" for the purpose of providing accurate timing information whenever the processor simulator interacts with the hardware simulator.

6. **Regarding dependent claims 2, 8 and 14**:

- The design verification method for microprocessors as claimed in claim 1, wherein, in the step of generating the **pipeline simulator**, a **source program** of the **pipeline simulator generated** by the **computer** based on the **pipeline specification** and a **source program** of a **simulator** independent of the **pipeline specification** are input, and the **pipeline simulator** is **generated** based on **both the source programs**.

Stapleton teaches a source program [source program, Col. 2, Line 40] of the simulator [executable program, Col. 2, Line 43] generated [transformed, Col. 2, Line 42] by the computer [computer system, Col. 2, Line 44] based on the specification [a class of objects each representing a logic circuit, Col. 2, Line 15] and a source program [vector class, Col. 2, Line 48] of a simulator [functions and operators, Col. 2, Line 51] independent of the pipeline specification are input ["a class" and "second class", Col. 2, Line 15 and 47], and the pipeline simulator [method for simulating, Col. 2, Line 60] is generated [created, Col. 2, Line 40] based on both the source programs ["a class" and "second class", Col. 2, Line 15 and 47].

Stapleton does not teach **pipeline specification** and **pipeline simulator**.

Hellestrand teaches pipeline characteristics (17, Fig. 1) [**pipeline specification**] and pipeline simulator (611, Fig. 6) [**pipeline simulator]**

It would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Stapleton to include "pipeline specification and pipeline simulator" for the purpose of providing accurate timing information whenever the processor simulator interacts with the hardware simulator.

7. **Regarding dependent claims 3, 4, 9, and 10**:

- The design verification method for microprocessors as claimed in claim 1, wherein, in the step of comparing the simulation results, it is **verified** that the **RTL description is correct** when both the result of the simulation of the RTL description and the result of the **pipeline simulation** are **agreed**.

Stapleton teaches comparing the simulation results, it is verified (Verify, Fig. 1) that the RTL description is correct (108 LOGIC Synthesis, Fig. 1) when both the result of the simulation of the RTL description and the result of the pipeline simulation are agreed (Verify, Fig. 1).

Stapleton does not teach **pipeline specification** and **pipeline simulator**.

Hellestrand teaches pipeline characteristics (17, Fig. 1) [**pipeline specification**] and pipeline simulator (611, Fig. 6) [**pipeline simulator**]

It would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Stapleton to include "pipeline specification and pipeline simulator" for the purpose of providing accurate timing information whenever the processor simulator interacts with the hardware simulator.

8. **Regarding dependent claims 5, 6, 11, 12, 15 and 16**:

- The design verification method for microprocessors as claimed in claim 1, the **pipeline specification** described in functions of **C++ language** is used.

Stapleton teaches the pipeline specification [RTL model, Col. 2, Line 40] described in functions of C++ language is used [object oriented programming language C++ is used, Col. 2, Line 38 – 39].

Stapleton does not teach **pipeline specification**.

Hellestrand teaches pipeline characteristics (17, Fig. 1) [**pipeline specification**] and pipeline simulator (611, Fig. 6) [**pipeline simulator**]

It would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Stapleton to include "pipeline specification and pipeline simulator" for the purpose of providing accurate timing information whenever the processor simulator interacts with the hardware simulator.

9. **Regarding Independent claims 7 and 13**:

- An **input section** for inputting a **pipeline specification of a microprocessor as a target in design** described in a **description language readable and analyzable by a computer**;

Stapleton teaches "a logic circuit **[specification of a microprocessor as a target in design]** representation which includes executable code **[description language readable and analyzable by a computer]**" that can be linked into **[input section]** a computer-aided design tool for simulation or verification. (Col. 1, Line 26 – 29)

- A **simulator generation section** for **generating** a **pipeline simulator** by the computer based on the **pipeline specification input through the input section**;

Stapleton teaches a "103 COMPILE" block **[simulator generation section]** for generating a "104 SIMULATE" block [**generating** a **simulator**] based on "102 C++ MODEL" [**specification input through the input section**]; (Fig. 1)

- A **program generation section** for **generating verification programs** by the computer based on the **pipeline specification** input through the input section;

Stapleton teaches a "106 CONVERT TO VERLOG MODEL" block [**program generation section**] for generating "106 VERLOG MODEL" [**generating verification programs**] based on the "102 C++ MODEL" [**specification**]. (Fig. 1)

- A **RTL simulation execution section** for **executing a pipeline simulation** of **a RTL description** based on the **verification programs** generated by **the program generation section** and the ***RTL* description of the microprocessor**;

Stapleton teaches a "107 SIMULATE" [**RTL simulation execution section**] for "107 SIMULATE" [**executing a simulation**] of "102 C++ MODEL" [**RTL description**] based on the "VERILOG MODEL" [**verification programs**] generated by "106 CONVERT TO VERILOG MODEL" [**program generation**

section] and the "C++ MODEL" [***RTL* **description of the microprocessor**]. (Fig. 1)

Further, Stapleton teaches a register transfer level (RTL) model [**RTL description**] is created using an object-oriented programming language [**C++**]. (Line 1 – 2, Abstract)

- A **pipeline simulation execution section** for **executing a pipeline simulation** based on the **verification programs** generated by the **program generation section** and the **pipeline simulator** generated by the **simulator generation section**;

Stapleton teaches a "104 SIMULATE" [**simulation execution section**] for "104 SIMULATE" [**executing a simulation**] based on "107 SIMULATE" [**verification programs**] generated by the "106 CONVERT TO VERILOG MODEL" [**program generation section**] and the "104 SIMULATE" [**simulator**] generated by "103 COMPILE" [**simulator generation section**]. (Fig. 1)

- A **comparison section** for **comparing** a **result of the simulation** executed by the **RTL simulation execution section** and a **result of the pipeline simulation** executed by the **pipeline simulation execution section**, and **verifying** an **operation of the pipeline of the microprocessor** based on a **comparison result**.

Stapleton teaches a "105 VERIFY" [a **comparison section**] for "VERIFY" [**comparing**] a result of the simulation executed by "107 SIMULATE" [**RTL simulation execution section**] and a result of the simulation executed by the "104 SIMULATE" [**simulation execution section**], and "105 VERIFY" [**verifying** an **operation of the of the microprocessor**] based on a "105 VERIFY" [**comparison result**]. (Fig. 1)

Stapleton does not teach **pipeline specification** and **pipeline simulator**.

Hellestrand teaches pipeline characteristics (17, Fig. 1) [**pipeline specification**] and pipeline simulator (611, Fig. 6) [**pipeline simulator**]

It would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Stapleton to include "pipeline specification and pipeline simulator" for the purpose of providing accurate timing information whenever the processor simulator interacts with the hardware simulator.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wile (U.S. Patent No. 6,327,559) discloses Pipeline Behavioral, Simulation control, testing and verifying a design for microprocessor logic. Mark Heinrich et al. (Hardware/software Codesign of the Stanford Flash Multiprocessor, IEEE, 1997) discloses pipeline simulator, RTL, ISA, Coupling. Herbert Grunbacher et al. (WinDLX and MIPSim Pipeline Simulators for Teaching Computer Architecture, IEEE, 1996) discloses pipeline simulator, behavior.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sunray Chang whose telephone number is 703-305-8744. The examiner can normally be reached on M-F 7:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Anthony Knight can be reached on (703)308-3179. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-746-3506.

Sunray Chang
Patent Examiner
Group Art Unit 2121
Technology Center 2100
U.S. Patent and Trademark Office

June 30, 2004

Anthony Knight
Supervisory Patent Examiner
Group 3600